A ROBUST DIGITAL TIMING RECOVERY WITH ASYMMETRY COMPENSATOR FOR HIGH SPEED OPTICAL DRIVE SYSTEMS

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Abstract - This paper presents a new four-sampled zero crossing asymmetry compensation algorithm for high-speed DVD/CD applications. Simulations show 34% improvement of jitter performances, 50% reduction of compensation time and 2.0dB gain of Bit Error Rate (BER) compared with other algorithms. Simultaneously, a new digital timing recovery scheme for the optical drive system is presented. By comparative simulations using DVD patterns with marginal input conditions, the proposed timing recovery algorithm shows enhanced performances in jitter variance and SNR margin by 4 times and 3dB respectively.

I. INTRODUCTION

The advent of the multimedia age brings on enormous demand for storage and transmission of high-capacity digital data. The successor of the original CD standard, designated as DVD, expands storage capacity by roughly an order of magnitude compared to that of CD. The first DVD system holds 4.7 GBytes and there is a great deal of research in developing a high-density DVD system up to 17 GBytes [1][2][3].

In receivers for such optical storage systems, proper symbol timing recovery is of crucial importance for good system performance. Poor synchronization has an effect on the fidelity of the sample values which are used for data detection. Therefore extension of data capacity depends upon accurate timing synchronization. The conventional DVD systems adopted analog timing recovery. Recently, however, high speed DVD systems are implemented digitally. In the past, data-aided timing recovery technique originated from the work of Mueller & Muller [4] and Gardner [5], has been developed for high density recording. The classical paper of Mueller and Muller describes baud rate timing recovery schemes that force a prescribed timing function toward zero. In order to strengthen the function for high density storage system, we consider the high speed digital DVD systems considering various channel effects such as bulk delay, asymmetry, and noise. In particular, the DVD-ROM/RAM 20X, where the sample rate is 523.2MHz and the frequency range of the sample rate is from 261.6MHz to 784.8MHz (wide range: ±50%) is considered. In this paper, we investigate timing recovery issues for various sampling
detector, and propose the suitable timing error detector and optimal timing control loop factor for high speed DVD systems.

The paper is organized as follows. In section II, the DVD system descriptions consisting of transmitter, channel modeling, and receiver are explained. In section III, asymmetry compensation method for improving the jitter performance and compensation time using four-sampled zero crossing algorithm is proposed and evaluated. In section IV, timing recovery scheme using proposed timing error detector is proposed and evaluated. In section V, the combined performance of the two proposed methods, which are asymmetry compensation and timing control loop are proposed. Finally, Conclusion is given in section VI.

II. SYSTEM DESCRIPTION

A. Transmitter model

In figure 1, the data source emits a bit sequence dω of data rate 1/Tω. This sequence represents the information that is to be conveyed. The digital data is coded before being stored on disc. This coded data is called channel data, and usually conforms to run-length-limited (RL.l) modulation codes. RLL codes are characterized by a d and a k constraint. These constraints signify that the shortest allowable domain recorded on disc comprises d+1 channel bit-intervals, while the longest domain comprises k+1 channel bit-intervals. A d=2, k=10 RLL code is used in the DVD standard [6]. A domain com-promising m channel bit-intervals is denoted by Im. Both user and channel sequences are assumed to take values from {−1, 1}.

B. Channel model

The channel model is composed of the three elements: the domain bloom, modulation transfer function (MTF), and optical pick-up (OPU) nonlinearity. The MTF is defined in the literature to be the same as the conventional transfer function except when the input is assumed to be a rectangular pulse. After feeding RLL (2,10) NRZI data into this channel model, we can get the waveform that is similar to the output signal of the real optical channel.

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In the system, the trigonometric channel model is adopted, since it has been commonly used in optical systems [7]. Eq. (1) shows the trigonometric channel model that has been proposed by Sony & Philips.

\[
H(f) = \frac{2}{\pi} \left( \cos^{-1}(f) - f \sqrt{1 - f^2} \right), \quad 0 \leq f \leq 1
\]

where, ‘f’ (value range between 0 and 1 inclusive) is the normalized frequency by the cutoff frequency \(F_{\text{cub}}\) of channel. Eq. (2) represents the cutoff frequency \(F_{\text{cub}}\) of the channel.

\[
F_{\text{cub}} = \frac{2 NA}{\lambda} |v| \quad \text{(Hz)}
\]

where, ‘v’ is the line-velocity of scanning-optical stylus, ‘NA’ is the numerical aperture of object lens, and ‘\(\lambda\)’ is the wavelength of laser. Figure 2 shows the impulse response of the trigonometric model.

Asymmetry is caused by several major factors like domain bloom [6][7], optical pickup nonlinearity, and some defects on disc themselves. In a read channel of optical disc systems such as DVD/CD, asymmetry or domain bloom is an imperfection in the disc which is due, among other factors, to under- or over-etching during the mastering process and which causes pits to be systematically too large or too small as in figure 3(a) and (c). On poorly manufactured discs, this phenomenon can cause pit-to-land and land-to-pit transitions to shift by a large fraction of the length of a single bit. Asymmetry phenomena can be explained as a ratio between center of long T (more than 6T) and 3T [6][7]. These unwanted asymmetry creations are getting much worse in the high-speed DVD/CD applications. The domain bloom is an inaccurate length of pit/land, so it can be modeled by assigning proper lengths of pit/land in NRZ signal as in figure 4. It is modeled by

\[
y(t) = \sum_{k=1}^{\infty} b_k g(t - (k + \Delta_k)T)
\]

where \(b_k\) is the transition sequence such as \(a_{k-1} a_k\) and \(g(t)\) is the transition response [7]. The displacement \(\Delta_k\) is a random variable that is statistically independent of \(a_k\) and \(b_k\). Eq. (3) can be approximately rewritten as

\[
y(t) \equiv \sum_{k} b_k g(t - kT) - T \sum_{k} b_k \Delta_k g'(t - kT)
\]

where \(b_k \Delta_k\) is a random noise sequence. Also, the term \(b_k g(t - kT)\) of eq. (4) can be rewritten as

\[
b_k g(t - kT) = \left( a_{k-1} - a_k \right) g(t - kT) = a_k h(t)
\]

Therefore, signal distortion due to asymmetry can be modeled as additive noise, and the variance of input signal \(b_k \Delta_k\) for transition jitter \(V(t)\) is given by \(\sigma^2 T \sigma^2\).

The extent of inaccurate length of pit/land is measured by a quantity known as signal asymmetry (ASM) and is defined as [6]:
\[ ASM = \frac{2 I^U_{k+1} + I^L_{k+1} - I^U_{k+1} + I^L_{k+1}}{2 I^U_{k+1} - I^L_{k+1}} \]  \hspace{1cm} (6)

where \( I^H_{k+1}, I^L_{k+1} \) stand for the high- (land) and low-peak (pit) amplitude values of the longest run \( I_{14} \) in DVD, and \( I^H_{k+1}, I^L_{k+1} \) for the high- and low-peak amplitude values of the shortest possible run \( I_3 \) in DVD. It is noticeable that the longest run in the DVD format is an \( I_{14} \) and not an \( I_{11} \), as the \( k=10 \) constraint would imply. This is due to the synchronization patterns, which do not correspond to coded user data (and thus do not necessarily follow the code constraints), and which contain \( I_{14} \) runs.

C. DVD reproducing apparatus: Receiver model

A receiver in DVDR system shown in figure 1 operates on the channel output \( r(t) \) to reproduce decision \( \hat{d}_a \) with respect to the data symbols \( d_a \). To this end it first converts \( r(t) \) into a discrete-time sequence \( n_k \) at the data rate \( 1/T \). The decision value is the combined result of all operations that precede decoder, detector, and demodulation including suppression of out-of-band, equalization of the data spectrum [7]. These preceding steps are beyond the scope of this paper. We concentrate on the digital timing recovery and asymmetry compensator. A sampling operation at instants \( t=nkT \) is synchronous with the transmitted data \( a_n \). This synchronization does not come for free but must be established by means of a separate timing-recovery subsystem. Timing recovery is critical to the performance of the receiver and is covered in detail in section IV. In figure 1, the input signal of ADC can be written by

\[ r(t) = \sum_{i=-\infty}^{\infty} b_i \cdot g (t - (i + \Lambda_i)T + \theta) + n(t) \]  \hspace{1cm} (7)

where \( b_i \) is the transition sequence such as \( a_i - a_{i-1} \) and \( g(t) \) is the transition response, \( \Lambda_i \) is an asymmetry due to the domain bloom, and \( \theta \) is a timing phase offset. The quantity denoted by \( n(t) \) is AWGN with noise spectral density \( N_0/2 \); therefore, \( n(t) \) is a circularly symmetric, zero-mean Gaussian random process with covariance function

\[ E[n(t)n(\tau)] = N_0 \delta(t-\tau) \]

If the frequency of the input data is the same as the frequency of the local oscillator, the sampled signal of the ADC can be expressed by

\[ n_k = r(t)_{|_{t=kt}} = b_k \cdot g (\theta - \Lambda_k T) + n'(kt) \]  \hspace{1cm} (8)

\[ n'(kt) = \sum_{i=k} b_i \cdot g ((k - i - \Lambda_i)T + \theta) + n(kt) \]  \hspace{1cm} (9)

assuming that the noise sample \( n(kt) \) has the same statistics as \( n(t) \). However, if the frequency of the input data \( T \) is not the same as the frequency of the local oscillator \( T_0 \), the sampled signal of the ADC can be expressed by

\[ r_k = r(t)_{|_{t=kt}} = b_k \cdot g \{k(T_0 - T) - \Lambda_k T + \theta\} + n'(kt) \]  \hspace{1cm} (10)

\[ n'(kt) = \sum_{i=k} b_i \cdot g \{(kT_0 - iT) - \Lambda_k T + \theta\} + n(kt) \]  \hspace{1cm} (11)

where \( T_0 - T \) is the timing frequency offset that is written by \( f_0 = f_a - f_0 \).

III. ASYMMETRY COMPENSATOR

In this paper asymmetry models mainly are focused on domain bloom and random jitter to characterize compensation time and jitter performances. In order to check the performance gain, three-sampled zero crossing (ZC 3 sample) [9], Digital Sum Value (DSV) [8], and proposed four-sampled zero crossing algorithm (ZC 4 sample) are considered. ZC 3 sample
method detects zero crossing points by examining each positive and negative sample values right near the zero crossing points. Then, the less absolute value out of previously detected two samples is selected. Instead of detecting zero crossing level, in DSV algorithm it just accumulates the polarities of all the sampled data (+1 or −1) over a zero level to decide the asymmetric errors. In contrast to other algorithms introduced above, the proposed algorithm uses four-sampled data instead of three-sampled one (ZC 3) or sums of all samples’ polarities (DSV). The proposed algorithm as shown in figure 5 consists of compensator (adder), zero crossing detector, asymmetry polarity detector, polarity counter, comparator, asymmetry error generator, integrator, and data detector. As shown in figure 6 when a signal crosses zero level with a negative slope, four-sampled zero crossing detector takes the two nearest samples \((D_{2k}, D_{3k})\) out of four samples \((D_{1k}, D_{2k}, D_{3k}, D_{4k})\) to make a decision for zero crossings. When there is a zero crossing, the ASM polarity detector decides polarities out of two outermost samples \((D_{1k}, D_{4k})\); the same manner applies for the positive zero crossing slope. In what follows, we will represent this scheme as a combination of formal algorithm and numerical formula. In Eq. (4), asymmetry error signal \(e_i(t)\) in the form of a periodically time-varying DC offset caused by asymmetry can be expressed by

\[
e_i(t) = -T \sum_{i=1}^{n} b_i \Delta g_i(t - iT).
\]

(12)

The decision of asymmetry polarity is achieved by each sample \(D_{1k}(t), D_{4k}(t)\) sum value, where, \(D_{1k}(t)\) and \(D_{4k}(t)\) can be written by

\[
D_{1k} = D_{1k}(t)_{\text{ext}} = a_{1k} h(k(T_n - T) + \theta) \pm T b_{1k} \Delta g_i((k - i)T) + n(kT)
\]

\[
D_{4k} = D_{4k}(t)_{\text{ext}} = a_{4k} h(k(T_n - T) + \theta) \mp T b_{4k} \Delta g_i((k - i)T) + n(kT)
\]

(13)

(14)

From Fig. 5, 6, and 7, we can summarize the following algorithm of asymmetry compensation with mathematical representation as follows.

**Step1. Asymmetry Polarity Decision**

If (ASM Polarity Detector = \(D_{1k} + D_{4k} > 0\))

{ Negative Asymmetry Counter -- }

Else

{ Positive Asymmetry Counter ++ }

**Step2. Asymmetry Compensation Decision**

If (Sum Counter = Positive ASM Counter + Negative ASM Counter > Positive threshold)

\[ y(t) = \sum_{i=-\infty}^{\infty} a_i h(t) - e_i(t) + c_i(t), \text{ Sum Counter} \rightarrow 0 \]

Else

\[ y(t) = \sum_{i=-\infty}^{\infty} a_i h(t) - e_i(t) + c_{i+1}(t) \]

If (Sum Counter = Positive ASM Counter + Negative ASM Counter > Negative threshold)

\[ y(t) = \sum_{i=-\infty}^{\infty} a_i h(t) + e_i(t) - c_i(t), \text{ Sum Counter} \rightarrow 0 \]

Else

\[ y(t) = \sum_{i=-\infty}^{\infty} a_i h(t) + e_i(t) - c_{i+1}(t) \]

where, Asymmetry Compensator signal \(c_i(t) = \sum_{k=-\infty}^{\infty} c_{k+1}(t)\).
\( c_i(t) = \{-1, 1\} \)

**Step 3. Asymmetry Compensation is achieved Steady state**

\[ y(t) = \sum_{i=1}^{\infty} a_i h(t) + \lim_{t \to \text{steady}} (\pm e_i(t) \mp c_i(t)) = \sum_{i=1}^{\infty} a_i h(t). \]

If the sum of \( D1_i(t) \) and \( D4_i(t) \) is positive, the detector accepts it as a negative asymmetry error. And if the sum is negative, a positive asymmetry error is applied to the detector. In the case asymmetry error, +1 is added to the polarity counter if it is the positive asymmetry error and –1 is added to it for the negative asymmetry error respectively as the step 1. The polarity counter is accumulative until it reaches the threshold level to decide errors. Then the accumulated value is compared with the threshold values in the comparator followed by ASM error generator to generate errors based on the compared values as the step 2. Finally, the errors integrated in the integrator are added to asymmetric input signals. And these results are now compensated and ready to be sent out to the data detector as the step 3.

![Figure 8. Compensation time comparison for algorithms](image)

**Figure 8. Compensation time comparison for algorithms**

The proposed four-sampled zero crossing algorithm has strong reliability even when phase, frequency, and large amount of asymmetry errors are present because as seen in figure 6 it uses the outermost samples \( (D1_i, D4_i) \) from zero crossing sector instead of right near ones \( (ZC \text{ algorithm}) \) for asymmetry error detection. It is beneficial to reduce influences generated from timing error and noise (AWGN). Since DSV algorithm has to accumulate the sums of polarities (+1 or –1) for every sample, compensation timing takes several pssec longer than the proposed four-sampled algorithm as shown in figure 8. And some largely distorted asymmetric signals might produce random jitter around zero crossing levels. For this reason ZC 3 sample algorithm cannot achieve correct decision because it has to use the samples right near the zero crossing points.

![Figure 9. Steady state jitter performance for algorithms](image)

**Figure 9. Steady state jitter performance for algorithms**

Figure 9 shows the enhancement in steady state jitter performance of the proposed scheme over other algorithms. As the simulation results show, DSV and ZC 3 algorithms have very weak characteristics for extended amount of asymmetry, especially when asymmetry exceeds 15.6%. For 15.6% asymmetry error the proposed algorithm has reduced jitter over ZC 3 sample and DSV algorithm by about 34% and 22%, respectively.

**IV. TIMING RECOVERY**

In the past, the analog timing recovery and the analog data reproduction have been widely used in the read-channel device owing to its simple realization. These days digital timing recovery is required for the digital data processing in the read-channel in order to obtain less BER (Bit Error Rate) using digital data recovery algorithms. Figure 10 shows the block diagram of the timing and data recovery for optical drives (CD/DVD). In the digital timing recovery, the farrow structure of a cubic Lagrange interpolator is used as the interpolation filter [10]. The analog RF data is sampled by the ADC at the fixed frequency, and the interpolation filter calculates the expected phase-locked data according to the control signal from the offset calculator. Then the data detector generates the final digital data (one or zero) using phase-locked and DC-canceled samples [8]. In the data detector, various data reproduction algorithms can be used depending on the tradeoff between the performance and the cost. While the Freq. error detector is used to maintain the frequency of the interpolated samples within the pull-in range of the timing error detector, the timing error detector detects the remaining frequency and phase offset. Finally, the digital loop filter receives error signals from two error detectors and generates the control value to the offset calculator.
Figure 10. The block diagram of the proposed digital timing recovery for optical drives

Figure 11. Proposed timing error detector

A. Timing error detector

Figure 11 shows the proposed timing error detector in the digital timing recovery. The algorithm consists of the zero-crossing detector, error detector, and timing controller. Since the timing error detector converges to the position of T/2 in the steady state condition, the second interpolation filter in figure 11 performs generation of the data signal having zero-crossing point. The output of the zero-crossing detector is determined by the XOR of the sign bit between D1 and D2 that are sampled value of $n_k$ and $n_{k-1}$, respectively. In the timing error detector, the time index $T'$ is determined by the output of the zero-crossing detector. Moreover, the time index $T'$ is not constant because the period of the input signal can be changed from $3T$ to $14T$. We can write that $T' = xT$, where the variable $x$ is an unknown random variable. Then, we can express the output of the error detector as follows:

$$
e_i = \frac{a_i}{4} \cdot \left( (D_{1i} - D_{1i-1}) + (D_{2i} - D_{2i-1}) \right)$$

where the variable $a_i$ is a quantized value of the $D_{1i-1}$.

The operating time index is changed from the period of the error detector $T'$ to the sample rate $T$ by the timing controller. And the timing controller consists of IIR filter shown in figure 11. The output of the timing controller is given by

$$z_k = e_i \times G^m$$

where the index $k$ is $l \cdot T' + m \cdot T$ ($l$ and $m$ are integer).

The sum of the timing controller during the one period of the error detector is given by

$$Z = e_i \times \frac{1}{1-G}$$

where the gain of the timing controller (IIR filter) is $1/(1-G)$.
The mean (s-curve) of the proposed timing error detector is shown in Figure 3 with that of the previous algorithms [4][5]. The s-curve can be represented by
\[ g(\phi) = E\left[z^1|\phi, \Delta f = 0\right] \] (18)
where \( \Delta f \) is a timing frequency offset and \( \phi = \theta - \hat{\theta} \) is a timing phase offset. The result of the figure 12(a) indicates that all the s-curves are almost same. Therefore, in the closed loop timing recovery, the tracking process using the proposed timing error detector is the same as other algorithms.

Figure 12(b) shows the variance of the timing error detector. The variance can be represented by
\[ \text{var}(\phi) = E\left[z^2|\phi, \Delta f = 0\right] - g^2(\phi). \] (19)

Since the variance of the proposed algorithm is almost 1/4 of that of the previous algorithms, the improvement in the jitter characteristic is expected. Therefore, in the closed loop timing recovery, the jitter of the steady state depends on the variance shown in figure 12(b). In the next subsection B, we describe the tracking process and jitter in more detail.

Figure 13. Equivalent model of the timing recovery

B. Closed-loop design

The equivalent model of the timing recovery is shown in figure 13. The timing phase error process is defined by [11]
\[ \phi_k = 0, \quad k = 0 \] (20)
\[ \phi_k = \theta_k - K_v \sum_{i=0}^{k-1} y_i, \quad k > 0 \] (21)
where \( K_v \) is a gain of the NCO and since \( \phi_k = \theta_k - \hat{\theta}_k \), we can write as follows:
\[ \hat{\theta}_k = K_v \sum_{i=0}^{k-1} y_i. \] By using eq. (20) and (21), the difference equation is defined by
\[ \phi_k - \phi_{k-1} = \theta_k - \theta_{k-1} - (\hat{\theta}_k - \hat{\theta}_{k-1}) = \theta_k - \theta_{k-1} - y_{k-1} \] (22)
\[ (1 - z^{-1})\phi_k = (1 - z^{-1})\theta_k - K_v z^{-1} y_k \] (23)
\[ y_k = z^{-n} D(z)[K_d g(\phi_k) + n(k)] \] (24)
where \( z^{-n} \) is a bulk delay [12], and \( K_d \) is a gain of the timing error detector. The digital loop filter of the second-order timing recovery is a first-order filter with single pole and can be represented as
\[ D(z) = G_1 + \frac{G_2}{1 - z^{-1}}. \] (25)

By using eq. (22), (23), and (24), we can write as follows:
\[ \phi_k = \theta_k - \frac{K_v}{1 - z^{-1}} z^{-n} D(z)[K_d \phi_k + n(k)] \] (26)
where, without loss of generality, we can assume that \( g(\phi_k) \equiv 1 \). Consequently, by using eq. (22), (25), and (26), the transfer function of the timing error recovery is [13]
\[ H(z) = \frac{\hat{\theta}}{\theta} = \frac{K_v K_d G_1(z - 1) + K_d K_v G_2 z}{z^2(z - 1)^2 + K_v K_d G_1(z - 1) + K_d K_v G_1 z}. \] (27)
The tracking jitter of the steady state is given by [13]
\[ \sigma^2_j = \frac{1}{2\pi} \int_0^{2\pi} |H(\omega)|^2 S_\varphi(\omega) d\omega \] (28)
where \( S_\varphi(\omega) \) is a power spectrum of the noise given by eq. (19). Figure 14 depicts the tracking jitter of the steady state for the SNR. The result indicates that the jitter of the proposed algorithm is superior to other algorithms.

Figure 14. Jitter of the steady state for various timing error detector’s algorithm

In control loops, the stability has the prime importance, which depends on the loop bandwidth [12][13]. By changing the loop bandwidth, various PLL characteristics - the locking time, the pull-in range, and the steady-state jitter - can be controlled. In digital implementations, the pipelining technique is inevitable to realize the fast architecture. But the bulk delay in the control loop directly influences the stability of the control loop [12]. Without the asymmetry, the pull-in ranges of the digital timing recovery loop for various bulk delays are shown in figure 15. These results are obtained by the
simulation with the assumption that the DVD disc is read at 20x MAX (523.2 MHz). The amount of noise, asymmetry, and blank in the input signal are getting worse when the speed of the optical disc gets higher. Even though it is required to increase the loop bandwidth in order to enhance the loop performance, the pull-in range cannot be increased further when the bulk delay in the loop is greater than ten clock periods.

Figure 15. Pull-in range of the digital timing recovery for the bulk delay

V. SIMULATION

In this section, we assess the performance of the proposed timing recovery with asymmetry compensator. A computer simulation achieves the probability of acquisition failure and BER performance for various channels as well as system parameters.

Figure 16 shows the failure probability of acquisition in the boundary of pull-in range shown in figure 15 when the proposed timing detector and asymmetry compensator are used. Also the channel and system parameters are as follows: SNR is 17dB, phase offset is 0.25T, and bulk delay is 20T. Figure 16(a) is the failure probability of acquisition for various asymmetries when the loop bandwidth is 2.33MHz. And figure 16(b) is the failure probability of acquisition for various loop bandwidths when the asymmetry error is 6.6%. Figure 16(a) indicates that the failure probability of acquisition increases as the asymmetry increases. When the failure probability of acquisition is 10^{-2}, the margin of the pull-in range is 0.9 MHz between the value of asymmetric error of 27% and 3.3%. In other words, when the timing recovery is restarted due to the blank, the success probability of acquisition is decreased as asymmetry increases. The figure 16(b) indicates that the timing recovery with the small loop bandwidth is more stable in comparison to large loop bandwidth. Because the pull-in range shown in the figure 15 is not influenced for almost all loop bandwidths, it is safe to say that the loop bandwidth should be decreased in order to reduce the asymmetry and noise.

Figure 16. Probability of acquisition failure for various asymmetry and loop bandwidth

Figure 17 shows the BER performance for various timing detector algorithms when the DSV algorithm of the asymmetry compensator is used. In the performance comparison, only the timing error detector in the proposed timing recovery system has been changed. The results indicate that the proposed detector has the 3dB SNR margin compared to the zero-crossing Gardner algorithm [5] when the BER is 3\times10^{-3} and the asymmetry is 3.3%. Especially, as the SNR increases, the BER gap between the proposed algorithm and the Gardner algorithm increases remarkably. Even though the asymmetry exists in the input signal, the BER has changed slightly because of the ‘asymmetry compensator’ block in the figure 10.

Figure 18 shows the BER performance of the reproduced
digital data with the proposed digital timing recovery as shown in the figure 5, 7, 10, 11 when the proposed timing detector algorithm is used. The results indicate that the proposed asymmetry algorithm has the improved BER performances by 0.4dB for ZC3 and 2.0dB for DSV when the BER is $1 \times 10^{-3}$ and the asymmetry is 15.6%.

Figure 17. BER performance of the DVD systems for various timing detector algorithms when using DSV of asymmetry compensator

performances by 0.4dB for ZC 3 and 2.0dB for DSV in asymmetry error 15.6%. Also it shows about 50% reduction of asymmetry compensation time as well as 22% or 34% improvement against jitter with respect to DSV and ZC 3 algorithms. And these results still hold even for the large amount of asymmetry errors (above 15.6%), which are the key factor to measure the accuracy of the asymmetry detector.

Second, the digital timing recovery scheme for high speed optical drives is presented, and the proposed timing recovery scheme is compared with traditional algorithms. The proposed timing recovery has almost 1/4 of variance compared to the zero-crossing Gardner or M&M algorithm, and has the 3dB SNR margin compared to the zero-crossing Gardner algorithm when the BER is $3 \times 10^{-5}$ and the asymmetry is 3.3%. The pull-in range of the digital timing recovery has been tested for various bulk delays and loop bandwidths, and the simulation result shows that the bulk delay in the loop should be less than ten clock periods for the wide pull-in range. In order to reduce the effects of the asymmetry error and noise as well as the failure probability of acquisition due to blank, however, the loop bandwidth needs to be decreased.

In conclusion, the performance of the proposed receiver architecture with the proposed timing detector and asymmetry compensator algorithm is more satisfactory than the conventional structures with ZC Gardner/ZC 3 samples or ZC Gardner/DSV algorithm.

VI. CONCLUSION

First, in this paper, two common asymmetry compensation algorithms and the proposed four-sampled zero crossing methods are analyzed and compared based on the optical drive system. The simulation results show that the proposed four-sampled zero crossing algorithm has improved BER

REFERENCES


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